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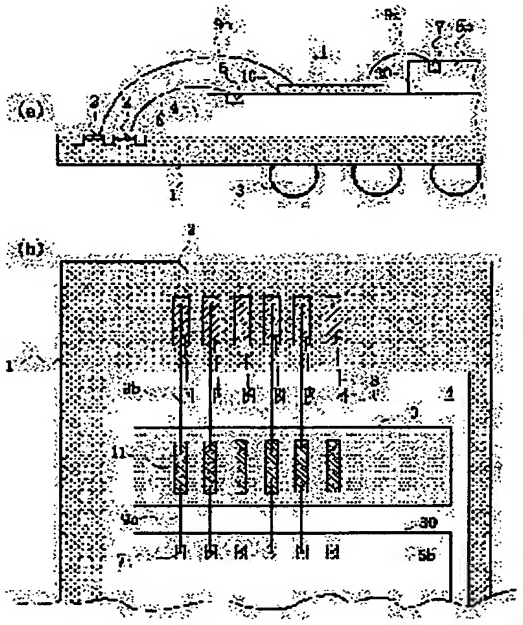
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device for varying the combination of semiconductor chips which can be assembled, and for facilitating a countermeasure to various demands at low costs by applying a general semiconductor chip, by preventing the occurrence of any electric short circuit due to the contact of any bent bonding wire with the other bonding wire or a semiconductor chip 4 in laminating and loading a plurality of semiconductor chips on a wiring board.

SOLUTION: An insulating tape material 10 in which a conductive member 11 of a relay means is formed is laminated on the main face of a first semiconductor chip 4. A bonding wire 9a is connected between the electrode pad 7 and the conductive member 11, and a bonding wire 9b is connected between the conductive member 11 and the wiring electrode 2. Therefore, the bonding wire can be relayed by the conductive member 11, and the wire bonding of a second semiconductor chip 5b can be realized by the two bonding wire 9a and 9b and the conductive member 11 formed of a copper foil or the like.



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CLAIMS

[Claim(s)]
[Claim 1] The 1st electrode pad formed in the front face of the 1st, the 2nd semiconductor chip, and said 1st semiconductor chip, and the 2nd electrode pad formed in the front face of said 2nd semiconductor chip, The lead terminal for external connection, and the 1st and the 2nd area for second bondings of said external connection lead, The 1st wire which connects said the 1st electrode pad and said 1st area, In the semiconductor device which possessed the 2nd wire which connects said the 2nd electrode pad and said 2nd area, superimposed said the 1st and 2nd semiconductor chip, and was closed in one package The semiconductor device characterized by forming the height of said 1st area low to said 2nd area.
[Claim 2] The semiconductor device according to claim 1 characterized by establishing the difference of said height by a part for the point of said lead terminal being bent caudad.
[Claim 3] The semiconductor device according to claim 1 characterized by bending a part for the point of said lead terminal twice [at least].

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which can be miniaturized also in the combination of a semiconductor chip with the approximated magnitude, piling up and carrying out the mold of two or more semiconductor chips.
[0002]
[Description of the Prior Art] The semiconductor device built into not knowing and these in the place in which small [to various electronic equipment] and the wave of lightweight-izing remain will also be expected much more large capacity, high efficiency, and high integration.
[0003] Then, in one package which existed as the way of thinking (for example, JP,55-1111517,A), the technique which closes two or more semiconductor chips attracted attention, and the implementation-ized motion came out from before. That is, as shown in drawing 5 (A), die bond of the 1st semiconductor chip 2 is carried out to the island 1 of a leadframe, the electrode pad and lead terminal 4 which fix the 2nd semiconductor chip 3 and correspond on the 1st semiconductor chip 2 are respectively connected with the 1st with the 2nd wire 5a and 5b, using a leadframe as a support material, and it closes by resin 6.
[0004]
[Problem(s) to be Solved by the Invention] However, when bonding of both 5a and the 1st and 2nd 5b was carried out to the front face of a lead terminal 4, there was a fault that both wire spacing LW tended to become narrow as shown in drawing 5 (B). When the wire spacing LW is narrow, as shown in drawing 5 (C), when the 1st and the 2nd wire 5a and 5b are crossed, in an intersection 7, it will be easy to cause short circuit accident, and the fall of the assembly yield will be caused. For this reason, the array of the electrode pad 8 and a lead terminal 4 had much constraint, and there was a fault that the degree of freedom of a design was small.
[0005]
[Means for Solving the Problem] This invention is what was accomplished in view of the conventional technical problem mentioned above. The 1st and the 2nd semiconductor chip, The 1st electrode pad formed in the front face of said 1st semiconductor chip, and the 2nd electrode pad formed in the front face of said 2nd semiconductor chip, Lead terminal for external connection The 1st and the 2nd area for second bondings of said external connection lead, The 1st wire which connects said the 1st electrode pad and said 1st area, In the semiconductor device which possessed the 2nd wire which connects said the 2nd electrode pad and said 2nd area, superimposed said the 1st and 2nd semiconductor chip, and was closed in one package It is characterized by forming the height of said 1st area low to said 2nd area.
[0006]
[Embodiment of the Invention] The gestalt of the operation of the 1st of this invention to the following is explained to a detail.
[0007] First, similarly the sectional view in which drawing 1 shows the principal part of the semiconductor device of this invention, and drawing 2 (A) are the sectional view showing the whole, and a top view in which drawing 2 (B) shows the whole.
[0008] In these drawings, 10 and 11 show the 1st and the 2nd semiconductor chip respectively. In the last process, much activity and a passive circuit element are formed in the silicon front face of the 1st and the 2nd semiconductor chip 10 and 11 of various kinds of diffusion heat treatments etc. The 1st [for external connection] and 2nd electrode pad 12a and 12b is formed in the chip circumference parts of the 1st and the 2nd

semiconductor chip 10 and 11 with the aluminum electrode. A passivation coat is formed on each electrode pads 12a and 12b, and opening of the upper part of the electrode pads 12a and 12b is carried out for electrical connection. Passivation coats are a silicon nitride, silicon oxide, a polyimide system insulator layer, etc. In the example of drawing 2 (B), each electrode pads 12a and 12b are collected and arranged along with two sides which semiconductor chips 10 and 11 counter.

[0009] Die bond of the 1st semiconductor chip 10 is carried out by adhesives 14 on the island 13 of a leadframe. The 2nd semiconductor chip 11 has fixed with adhesives 15 on said passivation coat of the 1st semiconductor chip 10. Adhesives 14 are epoxy system adhesives conductive or insulating, and insulating in adhesives 15.

[0010] The end of 1st bonding wire 16a which consists of a gold streak is connected to 1st electrode pad 12a, and wire bond of the other end of 1st bonding wire 16a is carried out to the lead terminal 17 for external derivation. Moreover, wire bond of the end of 2nd bonding wire 16b is carried out to the front face of 2nd electrode pad 12b, and wire bond of the other end of 2nd bonding wire 16b is carried out to the lead terminal 17 for external derivation.
 [0011] The mold of some of the 1sts, 2nd semiconductor chips 10 and 11, lead terminals 17, and the principal part containing the 1st and the 2nd bonding wire 16a and 16b is carried out by the heat-curing resin 18 of an epoxy system in a perimeter, and they form the package of a semiconductor device. A lead terminal 17 is drawn from the side attachment wall of a package outside, and turns into an external connection terminal. Bending of the drawn lead terminal 17 is carried out to the Z character mold. It has exposed to the front face of resin 18, and the rear-face side of an island 13 forms the same flat surface as resin 18 front face.

[0012] The combination of the 1st and the 2nd semiconductor chip 10 and 11 is arbitrary. For example, when semiconductor memories, such as EEPROM (flash memory), are used as the 1st and the 2nd semiconductor chip 10 and 11 (1st example of combination), storage capacity can be made into ... 3 times twice with one package. Moreover, in semiconductor memories, such as EEPROM (flash memory), when forming semiconductor memories, such as SRAM, in the 2nd semiconductor chip 11 (2nd example of combination), things are also considered by the 1st semiconductor chip 10. For each chip, the I/O terminal which outputs and inputs data, and the address terminal which specifies the address of data and the chip enable terminal which permits I/O of data are provided, and, in [both of] the case of combination, the pin out of both chips resembles closely. Therefore, it is possible to share the I/O terminal of the 1st and the 2nd semiconductor chip 10 and 11 and the lead terminal 17 for address terminals, and it is possible by impressing an exclusive chip enable signal to each chip to choose the memory cell of one of semiconductor chips exclusively.

[0013] As for a lead terminal 17, the front face is located in the height between the front face of the 1st semiconductor chip 10, and the front face of the 2nd semiconductor chip 11. It is bent at the bending include angle theta, and is a point, and a part for the point of a lead terminal 17 is lower part bending ******** about 150 micrometers. From the bent part to a tip is set to the 1st area 17a, and from the bent part to the edge of the resin 18 interior is set to the 2nd area 17b. If this bending is performed at the time of processing molding of a leadframe, it is simple.

[0014] And second bond of the 1st bonding wire 16a is carried out to the front face in the middle of [area 17a] the 1st, and second bond of the 2nd bonding wire 16b is carried out to the 2nd area 17b front face. By this, about 100 micrometers of height of the second bond point of 1st bonding wire 16a can be caudad located to the second bond point of 2nd bonding wire 16b. Therefore, the wire spacing LW between the 1st, and the 2nd bonding wire 16a and 16b is expandable.

[0015] Drawing 3 is the sectional view showing the gestalt of operation of the 2nd of this invention. It is the example which performed bending processing to lead terminal 17 point twice, and secured the levelness of 1st area 17a to the gestalt of previous operation. The same sign is lain down on the same part, and explanation is omitted. Lead terminal 17 point bends again from the part bent by the acute angle from the 2nd area 17b, and the part bent by the acute angle, and 1st area 17a extends in it. The include angle theta of the 1st area 17a front face can be eased rather than a previous example by having bent twice. This improves the bonder kinky thread tee at the time of the second bond of 1st bonding wire 16a.

[0016] The condition when performing second bond to drawing 4 to the lead terminal 17 which has such a bending part was shown. Drawing 4 (A) and (B) correspond to the gestalt of the 2nd operation of drawing 4 (C) and (D) in the gestalt of the 1st operation respectively.

[0017] A heat coma 20 for heating bonding area is prepared for activity area at the time of wire bond, and the

irregularity according to bending of lead terminal 17 front face is formed in the front face of the heat coma 20. A lead terminal 17 is pressed so that the front face of a heat coma 20 may be contacted and the lead rear face of the 1st and the 2nd area 17a and 17b may stick a lead terminal 17 to heat coma 21 front face by the window clamper 21 with reference to drawing 4 (A) and (C). Wire bond of the 1st and the 2nd bonding wire 16a and 16b is performed heating by the heat coma 20 in this condition. And the window clamper 21 is released and wirebonding is ended. At this time, a lead terminal 17 returns to the original configuration by being released from press.

[0018]

[Effect of the Invention] Since it considered as the configuration which established the 1st area and 2nd area in lead terminal 17 point, and lowered the height of the 1st area caudad according to this invention as explained above, the wire spacing LW of the 1st and the 2nd bonding wire 16a and 16b is expandable. It has the advantage which can prevent electric short circuit accident when a crossover is located in a wire by this.

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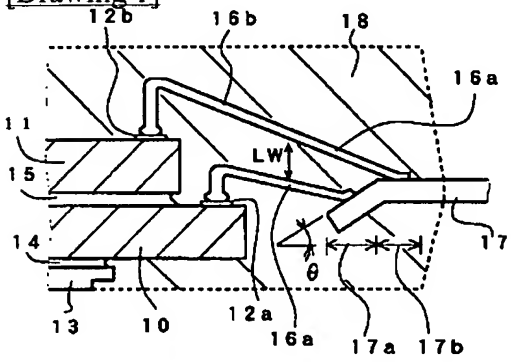
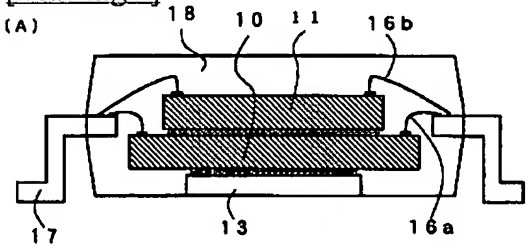
DRAWINGS

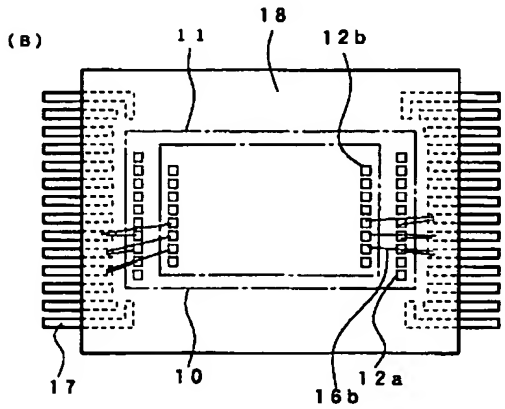
[Drawing 1]



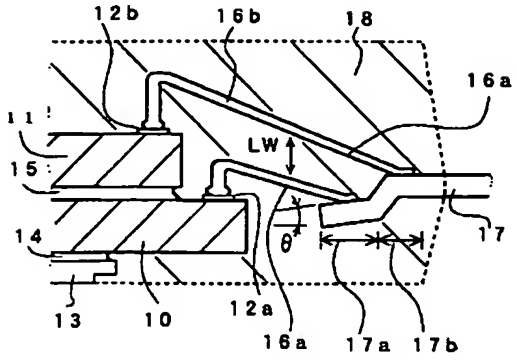
10 第1の半導体チップ
11 第2の半導体チップ
12a第1のボンディングパッド
12b第2のボンディングパッド
13 アイランド
16a第1のボンディングワイヤ
16b第2のボンディングワイヤ
17 リード端子
18 樹脂

[Drawing 2]

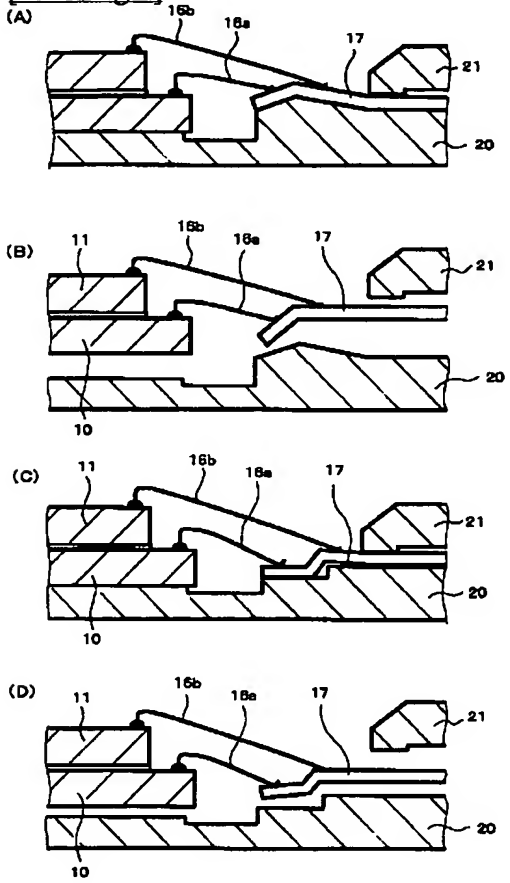




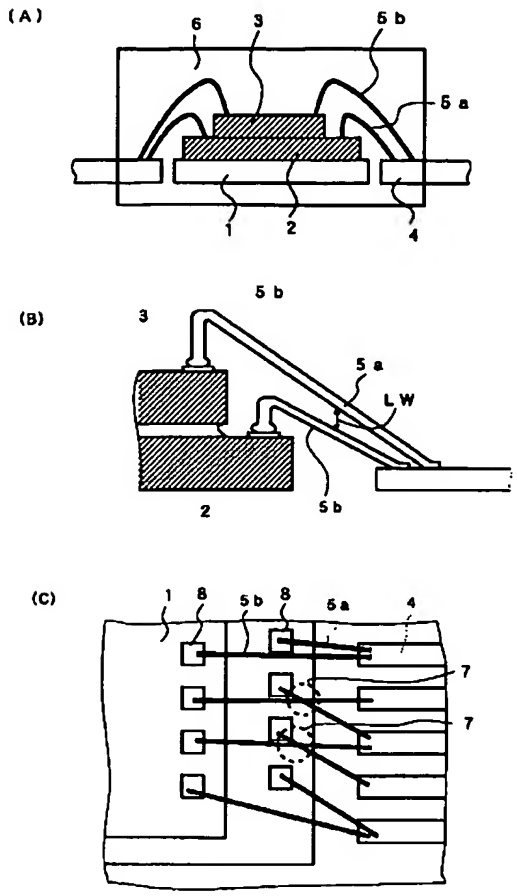
[Drawing 3]



[Drawing 4]



[Drawing 5]



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